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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,380	11/14/2003	Xin M. Wu	ITL.1049US (P17703)	1611
21906	7590	09/27/2006	EXAMINER	
TROP PRUNER & HU, PC 1616 S. VOSS ROAD, SUITE 750 HOUSTON, TX 77057-2631			VAN ROY, TOD THOMAS	
			ART UNIT	PAPER NUMBER
			2828	

DATE MAILED: 09/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/713,380	Applicant(s) WU ET AL.	
	Examiner Tod T. Van Roy <i>r. yee</i>	Art Unit 2828	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 August 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

The examiner acknowledges the amending of claims 1, 7, 12, and 17, as well as the addition of claims 22-23.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 7, 12, 17, and 22-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 1, 7, 12, 17, and 22-23 are believed to contain new matter not presented with the applicant's disclosure. Each of these claims describes a pair of series connected resistors to be found in the described circuit. None of the figures, or the specification, teach resistors connected in a series configuration. Figure 5 of the applicant's specification is found to teach two pairs of resistors, each pair being formed in a parallel configuration. If, for arguments sake, the applicant had intended to claim a parallel configuration, the claims would still present new matter when dependent claims 6, 11, 15, and 20 are taken into account (as these claims would present multiple parallel resistor configurations). As the Remarks (submitted 08/04/2006) failed to explain the

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new claim limitations, the examiner is of the belief that the presented amendments constitute new matter.

An updated search has been performed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4, 7, 9, 12, 14, 17, 19, and 22-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Taguchi (US 6320890).

With respect to claims 1 and 22, Taguchi discloses a method comprising: providing current to a laser diode of an optical communication system (transmitter-diode, receiver-storage media) using a transistor (fig.10 #74) coupled in series with said laser diode (fig.10 LD) between a power supply voltage (fig.10 Vcc) and ground, and providing a first and a second resistance (fig.10 #R5/R6), the ratio of the first to the second resistance being a matching resistance (can be any value) and the first and the second resistances are both greater than said matching resistance (*Taguchi does not disclose resistance values for R5 or R6 (R4 taught to be at least 100 ohms, col.10 lines 42-45) however, it is inherent that the resistance values would be greater than 1 ohm as the circuit would essentially act as if the resistors were not present otherwise, hence*

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there are 3 scenarios: (1) the resistance values are equal making the matching value 1, and less than R5 and R6 (2) R5 is larger than R6, then R6 will be designated the "first" and R5 the "second" resistance, making the ratio of the "first" to the "second" less than either R5 or R6 (3) R6 is larger than R5, then R5 will be designated the "first" and R6 the "second" resistance, making the ratio of the "first" to the "second" less than either R5 or R6; thus for any reasonable scenario the resistors of Taguchi meet the claim limitation).

With respect to claim 2, Taguchi discloses providing a differential output stage (fig.10, formed of: R5, R6, #71,73) coupled to drive said transistor (col.11-12 lines 49-4).

With respect to claim 4, Taguchi discloses the transistor to be base driven (fig.10 #74, differential output connected to base).

With respect to claims 7 and 23, Taguchi discloses a method comprising: forming a direct modulation laser driver including a transistor (fig.10 #74) coupled between a power supply (fig.10 Vcc) and a laser diode (fig.10 LD); and coupling said transistor to be driven by a differential output stage (fig.10, formed of: R5, R6, #71,73), and providing a first and a second resistance (fig.10 #R5/R6), the ratio of the first to the second resistance being a matching resistance (can be any value) and the first and the second resistances are both greater than said matching resistance (*Taguchi does not disclose resistance values for R5 or R6 (R4 taught to be at least 100 ohms, col.10 lines 42-45) however, it is inherent that the resistance values would be greater than 1 ohm as the circuit would essentially act as if the resistors were not present otherwise, hence there are 3 scenarios: (1) the resistance values are equal making the matching value 1, and*

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less than R5 and R6 (2) R5 is larger than R6, then R6 will be designated the "first" and R5 the "second" resistance, making the ratio of the "first" to the "second" less than either R5 or R6 (3) R6 is larger than R5, then R5 will be designated the "first" and R6 the "second" resistance, making the ratio of the "first" to the "second" less than either R5 or R6; thus for any reasonable scenario the resistors of Taguchi meet the claim limitation).

With respect to claim 9, Taguchi discloses the transistor to be a bipolar transistor (fig.10 #74) having its base coupled to said differential output stage.

With respect to claim 12, Taguchi discloses a driver for a direct modulation laser comprising: a differential output stage (fig.10, formed of: R5, R6, #71,73), a transistor driven by said differential output stage (fig.10 #74), said transistor coupled between a power supply (fig.10 Vcc) and ground, and a laser diode (fig.10 LD) coupled in series with said transistor, and providing a first and a second resistance (fig.10 #R5/R6), the ratio of the first to the second resistance being a matching resistance (can be any value) and the first and the second resistances are both greater than said matching resistance (*Taguchi does not disclose resistance values for R5 or R6 (R4 taught to be at least 100 ohms, col.10 lines 42-45) however, it is inherent that the resistance values would be greater than 1 ohm as the circuit would essentially act as if the resistors were not present otherwise, hence there are 3 scenarios: (1) the resistance values are equal making the matching value 1, and less than R5 and R6 (2) R5 is larger than R6, then R6 will be designated the "first" and R5 the "second" resistance, making the ratio of the "first" to the "second" less than either R5 or R6 (3) R6 is larger than R5, then R5 will be designated the "first" and R6 the "second" resistance, making the ratio of*

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the "first" to the "second" less than either R5 or R6; thus for any reasonable scenario the resistors of Taguchi meet the claim limitation).

With respect to claim 14, Taguchi discloses the transistor is a bipolar transistor (fig.10 #74) having a base coupled to said differential output stage (fig.10 #74, differential output connected to base).

With respect to claim 17, Taguchi discloses a system comprising: a media access control (fig.10 #57, would allow for control by a media device), a laser driver coupled to said media access control (fig.10), said laser driver including a differential output stage (fig.10, formed of: R5, R6, #71,73), a transistor driver by said differential output stage (fig.10 #74), said transistor coupled between a power supply and ground, and a laser diode (fig.10 LD) coupled in series with said transistor, and providing a first and a second resistance (fig.10 #R5/R6), the ratio of the first to the second resistance being a matching resistance (can be any value) and the first and the second resistances are both greater than said matching resistance (*Taguchi does not disclose resistance values for R5 or R6 (R4 taught to be at least 100 ohms, col.10 lines 42-45) however, it is inherent that the resistance values would be greater than 1 ohm as the circuit would essentially act as if the resistors were not present otherwise, hence there are 3 scenarios: (1) the resistance values are equal making the matching value 1, and less than R5 and R6 (2) R5 is larger than R6, then R6 will be designated the "first" and R5 the "second" resistance, making the ratio of the "first" to the "second" less than either R5 or R6 (3) R6 is larger than R5, then R5 will be designated the "first" and R6 the "second"*

resistance, making the ratio of the "first" to the "second" less than either R5 or R6; thus for any reasonable scenario the resistors of Taguchi meet the claim limitation).

With respect to claim 19, Taguchi discloses the transistor to be a bipolar transistor (fig.10 #74) having a base coupled to said differential output stage (fig.10 #74, differential output connected to base).

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 7-8, 12-13, and 17-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsai (US 2003/0156609).

With respect to claim 1, Tsai discloses a method comprising: providing current to a laser diode of an optical communication system (transmitter-diode, receiver-media which light strikes) using a transistor (fig.4 #Q501) coupled in series with said laser diode (fig.4 LD401) between a power supply voltage (fig.4 Vcc) and ground, and providing a first and a second resistance (fig.4 unlabeled near #VC2), the ratio of the first to the second resistance being a matching resistance (can be any value) and the first and the second resistances are both greater than said matching resistance (*Tsai does not disclose resistance values for R1 or R2 however, it is inherent that the resistance values would be greater than 1 ohm as the circuit would essentially act as if the resistors were not present otherwise, hence there are 3 scenarios: (1) the resistance values are equal making the matching value 1, and less than R1 and R2 (2) R1 is larger*

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than R2, then R2 will be designated the "first" and R1 the "second" resistance, making the ratio of the "first" to the "second" less than either R1 or R2 (3) R2 is larger than R1, then R1 will be designated the "first" and R2 the "second" resistance, making the ratio of the "first" to the "second" less than either R1 or R2; thus for any reasonable scenario the resistors of Tsai meet the claim limitation).

With respect to claim 2, Tsai discloses providing a differential output stage (fig.4, formed of: Resistor next to Q504, Resistor next to Q505, Q502, Q503) coupled to drive said transistor ([0034]).

With respect to claim 3, Tsai discloses the transistor to be gate driven (fig.4 Q501, differential output connected to gate).

With respect to claim 7, Tsai discloses a method comprising: forming a direct modulation laser driver including a transistor (fig.4 Q501) coupled between a power supply (fig.4 Vcc) and a laser diode (fig.4 LD401); and coupling said transistor to be driven by a differential output stage (fig.4, formed of: Resistor next to Q504, Resistor next to Q505, Q502, Q503), *(Tsai does not disclose resistance values for R1 or R2 however, it is inherent that the resistance values would be greater than 1 ohm as the circuit would essentially act as if the resistors were not present otherwise, hence there are 3 scenarios: (1) the resistance values are equal making the matching value 1, and less than R1 and R2 (2) R1 is larger than R2, then R2 will be designated the "first" and R1 the "second" resistance, making the ratio of the "first" to the "second" less than either R1 or R2 (3) R2 is larger than R1, then R1 will be designated the "first" and R2 the*

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"second" resistance, making the ratio of the "first" to the "second" less than either R1 or R2; thus for any reasonable scenario the resistors of Tsai meet the claim limitation).

With respect to claim 8, Tsai discloses the transistor to be a field effect transistor (fig.4 Q501) having its gate coupled to said differential output stage.

With respect to claim 12, Tsai discloses a driver for a direct modulation laser comprising: a differential output stage (fig.4, formed of: Resistor next to Q504, Resistor next to Q505, Q502, Q503), a transistor driven by said differential output stage (fig.4 Q501), said transistor coupled between a power supply (fig.4 Vcc) and ground, and a laser diode (fig.4 LD401) coupled in series with said transistor, *(Tsai does not disclose resistance values for R1 or R2 however, it is inherent that the resistance values would be greater than 1 ohm as the circuit would essentially act as if the resistors were not present otherwise, hence there are 3 scenarios: (1) the resistance values are equal making the matching value 1, and less than R1 and R2 (2) R1 is larger than R2, then R2 will be designated the "first" and R1 the "second" resistance, making the ratio of the "first" to the "second" less than either R1 or R2 (3) R2 is larger than R1, then R1 will be designated the "first" and R2 the "second" resistance, making the ratio of the "first" to the "second" less than either R1 or R2; thus for any reasonable scenario the resistors of Tsai meet the claim limitation).*

With respect to claim 13, Tsai discloses the transistor is a field effect transistor (fig.4 Q501) having a gate coupled to said differential output stage (fig.4 Q501, differential output connected to gate).

With respect to claim 17, Tsai discloses a system comprising: a media access control (fig.4 #412, would allow for control by a media device), a laser driver coupled to said media access control (fig.4), said laser driver including a differential output stage (fig.4, formed of: Resistor next to Q504, Resistor next to Q505, Q502, Q503), a transistor driver by said differential output stage (fig.4 Q501), said transistor coupled between a power supply and ground, and a laser diode (fig.10 LD) coupled in series with said transistor, *(Tsai does not disclose resistance values for R1 or R2 however, it is inherent that the resistance values would be greater than 1 ohm as the circuit would essentially act as if the resistors were not present otherwise, hence there are 3 scenarios: (1) the resistance values are equal making the matching value 1, and less than R1 and R2 (2) R1 is larger than R2, then R2 will be designated the "first" and R1 the "second" resistance, making the ratio of the "first" to the "second" less than either R1 or R2 (3) R2 is larger than R1, then R1 will be designated the "first" and R2 the "second" resistance, making the ratio of the "first" to the "second" less than either R1 or R2; thus for any reasonable scenario the resistors of Tsai meet the claim limitation).*

With respect to claim 18, Taguchi discloses the transistor to be a field effect transistor (fig.4 Q501) having a gate coupled to said differential output stage (fig.4 Q501, differential output connected to gate).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 5, 10, 16, and 21 rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi in view of Kwon et al. (US 2003/0002551).

With respect to claims 5, 10, 16, and 21, Taguchi teaches the lasers diode driver as outlined in the rejections to claims 1, 7, 12, and 17, but does not teach the use of an AC coupled matching resistor. Kwon teaches a laser diode driver that uses an AC coupled matching resistor (fig.3 Rc1). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the laser driver of Taguchi with the resistor of Kwon in order to reduce ringing during high speed operation (Kwon, [0030]).

Claims 6, 11, 15, and 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi in view of Tanaka et al. (US 2004/0114650).

With respect to claims 6, 11, 15, and 20, Taguchi teaches the lasers diode driver as outlined in the rejections to claims 1, 7, 12, and 17, but does not teach the use of parallel matching resistors. Tanaka teaches a laser diode driver which uses parallel

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matching resistors (fig.3 Rd). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the laser driver of Taguchi with the matching resistors of Tanaka in order to suppress the reflection of signals from the laser diode (Tanaka, [0040]).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.


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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tod T. Van Roy whose telephone number is (571)272-8447. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571)272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVR



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PRIMARY